Docket No.: J0658.0006
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jens Barrenscheen et al.

Application No.: 10/727,108 | Confirmation No.: 4414

Filed: December 2, 2003 | Art Unit: 2611

For: ARRANGEMENT COMPRISING A FIRST SEMICONDUCTOR CHIP AND A SECOND SEMICONDUCTOR CHIP CONNECTED THERETO | Examiner: J. F. A. Dsouza

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on August 10, 2009, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF. In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-2215.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.2:

I. Real Party In Interest
II Related Appeals and Interferences

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

INFINEON TECHNOLOGIES A.G.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 1-20 claims pending in application.

B. Current Status of Claims

1. Claims canceled: None
2. Claims withdrawn from consideration but not canceled: None
3. Claims pending: 1-20
4. Claims allowed: 17, 18, 20
5. Claims rejected: 1-16, 19

C. Claims On Appeal

The claims on appeal are claims 1-16, 19

IV. STATUS OF AMENDMENTS

Appellants filed a Response After Final Rejection on May 14, 2009, which did not amend the claims. The Examiner responded to the Response After Final Rejection in an Advisory Action mailed June 2, 2009. Accordingly, the claims enclosed herein as Appendix A incorporate the amendments indicated in the paper filed by Appellants on November 18, 2008.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is independent and claims 2-16 and 19 depend either directly or indirectly from claim 1. As shown below, each limitation of claim 1 is disclosed by at least the following citations to the Specification. Specification citations are provided in accordance with 37 C.F.R. § 41.37, such citations are merely examples of where support may be found in the specification. There is no intention to suggest in any way that the terms of the claims are limited to the examples in the specification or the specific citations used. As demonstrated by the reference numerals and citations above, the claims are fully supported by the specification as required by law. However, it is improper under the law to read limitations from the specification into the claims. The reference numerals and specification citations are not to be construed as claim limitations or in any way used to limit the scope of the claims.

Claim 1:

1. An arrangement (FIG. 2) comprising:

a first semiconductor chip (MCN) configured to transmit load control data and pilot data on a single line (SO) (pg. 8, ¶ [0039], lines 3-5; pg. 10, ¶ [0049]; pgs. 11-12, ¶ [0055]);

a second semiconductor chip (PCN) coupled to the first semiconductor chip (MCN) and configured to receive the load control data and the pilot data (pg. 8, ¶ [0039], lines 3-5; pg. 10, ¶ [0049]); and

a plurality of electrical loads coupled to the second semiconductor chip (PCN) (pg. 2, ¶ [0006] – pg. 3, ¶ [0010]);

wherein the second semiconductor chip (PCN) is configured to:

a) drive the plurality of electrical loads based on a timing that is defined by the load control data (pg. 2, ¶ [0008]; pg. 3, ¶ [0010]; pg. 7, ¶ [0039], line 3 - pg. 8, ¶ [0039], line 2),

b) transmit to the first semiconductor chip (MCN) diagnostic data (pg. 10, ¶ [0051]; pg. 15, ¶ [0069]), which represent at least one of a plurality of states of the second semiconductor chip (PCN) and events which occur in the second semiconductor chip (pg. 3, ¶ [0011]; pg. 8, ¶ [0039], lines 6-8), and

c) control a transmission rate of the diagnostic data as prescribed by the pilot data (pgs. 6-7, ¶ [0034]; pgs. 15-16, ¶ [0072]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The rejection of claims 1-4, 9-16 and 19 under 35 U.S.C. § 103(a) as being unpatentable over Arslain et al. (U.S. Patent No. 6,366,153) in view of Applicant Admitted Prior Art (hereinafter "AAPA") in further view of Ishii (EP 793111) and Flynn (U.S. Patent No. 5,525,971).

The rejection of claims 5-7 under 35 U.S.C. § 103(a) as being unpatentable over Arslain in view of the AAPA and in further view of Ishii, Flynn and Hastings et al. (U.S. Patent No. 6,772,251).[1]

The rejection of claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Arslain in view of the AAPA and in further view of Ishii, Flynn and Jeong (U.S. Patent No. 5,675,584).[2]

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[1] Appellants note that while the Final Office Action does not cite Flynn for the rejection of claims 5-7, for purposes of this appeal, Appellants presume Flynn is applied to in the rejection of these claims since claims 5-7 ultimately depend on claim 1.

[2] Appellants note that while the Final Office Action does not cite Flynn for the rejection of claim 8, for purposes of this appeal, Appellants presume Flynn is applied to in the rejection of this claim since claim 8 depends on claim 1.

VII. ARGUMENT

Claims 1-20 are pending and have been examined in the present application. Claims 1-16 and 19 stand rejected while claims 17, 18 and 20 have been allowed. Claim 1 is independent and claims 2-16 and 19 depend from independent claim 1. Appellant asserts that these claims stand improperly rejected under 35 U.S.C. § 103(a), and, therefore, respectfully submit that the board order the withdrawal of these rejections.

In particular, claims 1-4, 9-16 and 19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Arslain et al. (U.S. Patent No. 6,366,153) in view of Applicant Admitted Prior Art (hereinafter "AAPA") in further view of Ishii (EP 793111) and Flynn (U.S. Patent No. 5,525,971). Appellants respectfully submit that the rejection of each of the pending claims must be reversed for the following reasons.

To establish a prima facie case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or combine references to arrive at the claimed subject matter. The prior art references must also teach or suggest all the limitations of the claim in question. See M.P.E.P. § 706.02(j).

Here, the references, whether taken individually or in combination, do not disclose or suggest the invention claimed by Appellants. In particular, the prior art of record fail to disclose a "first semiconductor chip configured to transmit load control data and pilot data on a single line", as required by independent claim 1. Accordingly, the cited references fail to render obvious the claimed subject matter of claim 1.

The March 4, 2009 Final Office Action acknowledges at pages 3-4 that neither Arslain, AAPA nor Ishii disclose the transmission of load control data and pilot data on a single line, as required by independent claim 1. Rather, the Office Action cites Flynn for this limitation. In particular, the Office Action justifies its position arguing that Flynn discloses that load control data

and pilot data are transmitted on a single line citing column 5, lines 27-36 of Flynn. This conclusion is flawed for at least two reasons.

Firstly, Flynn discloses an external bus **80** that is 32 bits wide and that the VLSI tester uses this bus **80** as a 32-bit parallel access port. Flynn further states that an integrated circuit having a reduced width external bus (e.g., 16 or 8-bit external bus) can be used in an alternative embodiment. While the Office Action construes this teaching to reading on the claimed "single line" of independent claim 1, one of skill in the art would know that 8-bit busses enable parallel data transfer, which cannot be implemented using a single line.

Thus, while the Advisory Action asserts that "it is not inconceivable that one of skilled in the art can use time division multiplexing to transmit different types of data on a single", there is nothing in Flynn that even suggests this feature. Rather, it is clear based on Flynn's disclosure that external bus **80** (or a reduced width external bus) must transfer data in parallel to operate optimally. Accordingly, one of skill in the art would not know to further modify a "reduced width external bus" to read on the claimed "single line" of the instant application. Such conclusion is inconsistent with Flynn's use of a "parallel access port". (Emphasis added.)

Secondly, the Office Action argues that load control data and pilot data are both transmitted on Flynn's "reduced width external bus" **80**. However, the handshaking, control signals between VLSI tester and the test control **40** of integrated circuit **10** are transmitted via three separate lines on test control interface **90**. Specially, the E_RQ line, the E_RQT line, and the E_GT line are used to control the mode of test controller **40**. (See col. 5, line 54 et seq.) There is no indication that either load control data and/or pilot data are transmitted from the VLSI tester to the integrated circuit **10** via "reduced width external bus" **80**. Rather, "reduced width external bus" **80** is employed to facilitate DMA operation, for example.

Accordingly, for at least these reasons, Flynn fails to disclose or suggest "first semiconductor chip configured to transmit load control data and pilot data on a single line", as required by independent claim 1. Moreover, as acknowledged by the Examiner, neither Arslain, the

AAPA nor Ishii cure Flynn's deficiency. As such, the combination of prior art fails to arrive at the claimed subject matter of independent claim 1.

Accordingly, Appellants respectfully maintain their position that independent claim 1, along with its dependent claims, is patentable over the prior art of record. Appellants therefore respectfully request that the outstanding rejections be reversed and that this application is passed to issue.

Appellants further note that claims 5-8 depend directly from and contain all the limitations of independent claim 1. These dependent claims also recite additional limitations, which, in combination with the limitations of their respective independent claims, are neither disclosed nor suggested by the combination of Arslain, Ishii, the AAPA and Flynn. Accordingly, Appellants are not arguing these rejections separately from the arguments in response to the rejections of claims 1-4, 9-16 and 19, discussed above. As such, Appellants are therefore not required to submit a concise explanation for dependant claims 5-8. See 37 C.F.R. §41.37(c)(1)(v).

For the reasons discussed above, Appellants respectfully request that the board order the withdrawal of the rejections of pending claims 1-16 and 19.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendments filed by Applicants on November 18, 2009.

Dated: September 29, 2009

Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/727,108

1. An arrangement comprising:

a first semiconductor chip configured to transmit load control data and pilot data on a single line;

a second semiconductor chip coupled to the first semiconductor chip and configured to receive the load control data and the pilot data; and

a plurality of electrical loads coupled to the second semiconductor chip;

wherein the second semiconductor chip is configured to:

a) drive the plurality of electrical loads based on a timing that is defined by the load control data,

b) transmit to the first semiconductor chip diagnostic data, which represent at least one of a plurality of states of the second semiconductor chip and events which occur in the second semiconductor chip, and

c) control a transmission rate of the diagnostic data as prescribed by the pilot data.

2. The arrangement as claimed in claim 1, wherein the first semiconductor chip is a program-controlled unit.

3. The arrangement as claimed in claim 1 wherein the second semiconductor chip is a power chip.

4. The arrangement as claimed in claim 1, wherein the diagnostic data are transmitted in time with a transmission clock signal generated in the second semiconductor chip, and the transmission clock signal is not transmitted to the first semiconductor chip.

5. The arrangement as claimed in claim 1, wherein the transmission rate is prescribed by transmitting a division factor, and the second semiconductor chip divides the frequency of a transmission clock signal received from the first semiconductor chip by the division factor, and transmits the diagnostic data to the first semiconductor chip in time with the resultant transmission signal.

6. The arrangement as claimed in claim 5, wherein the transmission clock signal transmitted to the second semiconductor chip represents the transmission clock which is used by the first semiconductor chip to transmit the load control data or the pilot data to the second semiconductor chip.

7. The arrangement as claimed in claim 6, wherein the diagnostic data are transmitted in units of frames and each frame starts with a start bit having a prescribed value and ends with one or two stop bits having prescribed values.

8. The arrangement as claimed in claim 1, wherein the first semiconductor chip ascertains a phase of the diagnostic data by oversampling the diagnostic data.

9. The arrangement as claimed in claim 1, wherein the diagnostic data are transmitted via a line, which transmits neither the load control data nor the pilot data.

10. The arrangement as claimed in claim 1, wherein the load control data and the pilot data are transmitted via a transmission channel.

11. The arrangement as claimed in claim 10, wherein the transmission channel comprises:

a transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip;

a data line via which the first semiconductor chip transmits the load control data and the pilot data to the second semiconductor chip in time with the transmission clock signal; and

a chip select line via which the first semiconductor chip transmits a chip select signal to the second

semiconductor chip,

wherein said chip select signal indicates to the second semiconductor chip a start and end of data transmission intended for the second semiconductor chip via the data line.

12. The arrangement as claimed in claim 1, wherein the load control data and the pilot data are transmitted in units of frames and are transmitted using time-division multiplexing.

13. The arrangement as claimed in claim 12, wherein the first semiconductor chip defines time windows of constant length and transmits in each time window either a load control data frame or a pilot data frame or no data.

14. The arrangement as claimed in claim 13, wherein the first semiconductor chip transmits no further load control data frames for a respective length of n time windows after transmission of a load control data frame,

wherein $n \geq 0$ and n can be set by a user of the arrangement.

15. The arrangement as claimed in claim 14, wherein a pilot data frame can be transmitted only in a time window in which no load control data frame is transmitted.

16. The arrangement as claimed in claim 13, wherein transmission of the pilot data has priority when load control data and pilot data are awaiting transmission simultaneously.

17. An arrangement comprising

a first semiconductor chip and a second semiconductor chip connected thereto,

where the second semiconductor chip is additionally connected to electrical loads and drives these electrical loads on the basis of a timing which is defined by load control data,

where the first semiconductor chip transmits via a transmission channel to the second semiconductor chip the load control data and pilot data which control the second semiconductor chip,

where the transmission channel comprises:

a first transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip;

a second transmission clock line via which the first semiconductor chip transmits an inverse of the transmission clock signal to the second semiconductor chip;

a first data line via which the first semiconductor chip transmits the load control data and the pilot data to the second semiconductor chip in time with the transmission clock signal;

a second data line via which the first semiconductor chip transmits an inverse of the load control data and an inverse of the pilot data to the second semiconductor chip; and

a chip select line via which the first semiconductor chip transmits a chip select signal to the second semiconductor chip,

wherein said chip select signal signals to the second semiconductor chip a start and end of transmission of data intended for the second semiconductor chip via the data line,

where the second semiconductor chip transmits to the first semiconductor chip diagnostic data which represent at least one of states prevailing in the second semiconductor chip and events which occur in the second semiconductor chip,

wherein the first semiconductor chip includes means for transmitting appropriate pilot data to the second semiconductor chip, and the second semiconductor chip includes means for controlling a transmission rate by which the diagnostic data is transmitted to the first semiconductor chip in accordance with the appropriate pilot data.

18. The arrangement as claimed in claim 17, wherein output drivers on the first semiconductor chip, which output the load control data, the pilot data and the transmission clock signal, are LVDS drivers or other special drivers whose use allows electromagnetic interference to be kept down.

19. The arrangement as claimed in claim 1, wherein the first semiconductor chip has a plurality of output drivers configured to output the load control data, the pilot data and the transmission clock signal.

20. The arrangement as claimed in claim 17, wherein output drivers on the first semiconductor chip, which output the load control data, the pilot data and the transmission clock signal, are special drivers configured to minimize electromagnetic interference.

APPENDIX B

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

APPENDIX C

No related proceedings are referenced in II. above, hence copies of decisions in related proceedings are not provided.